High-Performance W-Band GaAs PIN Diode Single-Pole Triple-Throw Switch CPW MMIC

Michael Case, Mehran Matloubian, Hsiang-Chih Sun,
Debabani Choudhury, and Catherine Ngo
Hughes Research Laboratories, 3011 Malibu Canyon Road, Malibu, CA 90265 USA
Phone: (310) 317-5793, FAX: (310) 317-5483

Abstract

We present the device technology, design techniques, and circuit performance of a W-band single-pole triple-throw switch implemented in a coplanar waveguide (CPW) GaAs PIN diode MMIC technology. This switch provides more than 20 dB isolation and less than 1.5 dB insertion loss over the 75 to 85 GHz range, and more than 16 dB isolation and less than 1.6 dB insertion loss over the entire 75 to 110 GHz band. To our knowledge, this is the first report of a W-band CPW SP3T switch with state-of-the-art performance.

Introduction

Switching signals between ports is a critical function in many mm-wave systems such as RADAR, communications links, and electronically scanned antennae (ESAs). Most of these systems require switching to occur between an antenna and the transmit or receive circuitry. In such a location, the switch's insertion loss adds directly to receiver noise figure and reduces transmitter power; hence low insertion loss is an important characteristic for switches. Isolation is another very important characteristic that quantifies the leakage from an "on" to an "off" port.

PIN diodes are ideal for signal switching due to their low series resistance and parasitic capacitance. A microstrip single-pole single-throw (SPST) InP-based PIN diode switch MMIC with 25 dB isolation and 0.8 dB insertion loss at 85 GHz [1], and a microstrip SPST GaAs-based PHEMT switch MMIC with 22.5 dB isolation and 1.6 dB insertion loss at 94 GHz [2] have been demonstrated. However, the backside processing required for microstrip-based MMICs is costly and limits yield. Using CPW not only eliminates the need for backside processes, but makes the MMIC compatible with flip-chip mounting, further reducing the system cost.

GaAs PIN Diode MMIC Technology

The most important figure of merit for PIN diodes (or any device used as a switch) is it's cutoff frequency, $f_{PIN} = 1/2\pi R_{ON} C_{OFF}$, where R_{ON} is the on-resistance, and C_{OFF} is the off-capacitance. Good switch performance can be expected to about $1/10$ of this frequency. The cross-sectional diagram of a PIN diode is shown in figure 1. Many commercial PIN diodes use conductive substrates forcing the anode (for P-substrates) or cathode (for N-substrates) to ground. In this work we have used a semi-insulating substrate in order to fabricate low-loss CPW transmission lines. This requires us to make lateral contact to the cathode, which results in a series resistance slightly higher than would be obtainable with a vertical device.

0-7803-4603-6/97/$5.00 (c) IEEE

slightly higher than would be obtainable with a vertical device.

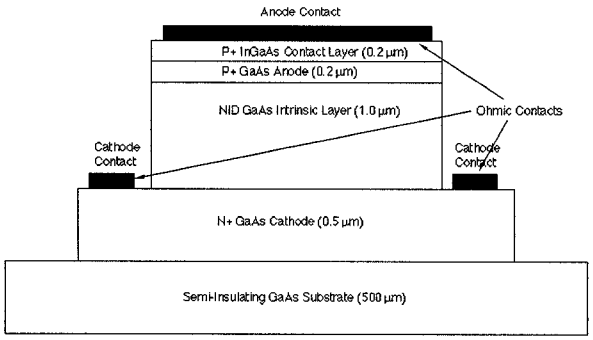

Figure 1. Cross sectional view PIN diode epitaxial structure. Off-state capacitance is determined by the not-intentionally doped (NID) I-layer dielectric constant and thickness. On-state resistance is dominated by parasitic ohmic contacts and spreading.

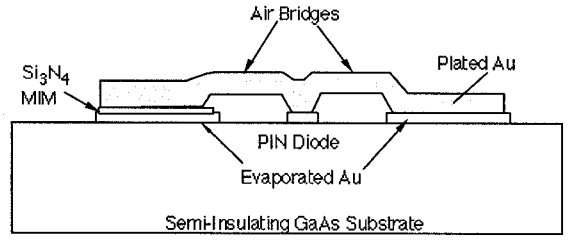

Figure 2. Cross sectional view PIN MMIC technology. The devices are complemented with Si_3N_4 MIM capacitors and plated Au air bridges.

When the diode is reverse-biased, the entire I-region is depleted, so the intrinsic off state capacitance (C_{OFF}) is determined by the material dielectric (GaAs ε_R = 12.9) and thickness. When the diode is strongly forward biased, the I-region presents minimal resistance since there is no intentional doping. Series resistance is dominated by parasitics (ohmic contact and spreading resistance through the cathode layer). Clearly, in order to maximize f_{PIN}, one should design the diode as a narrow stripe (just like FETs, HBTs, RTDs, etc.). For a 6 X 6 μm^2 device, R_{ON} = 5 Ω, C_{OFF} = 20 fF, f_{PIN} = 1.6 THz, and for a 6 X 10 μm^2 device, R_{ON} = 3 Ω, C_{OFF} = 33 fF, f_{PIN} = 1.6 THz (calculated, intrinsic parameters). Processing includes mesa etching to expose the cathode and to isolate devices, alloyed AuGe ohmic contacts, evaporated interconnect metal, PECVD Si_3N_4 for MIM capacitors, and finally plated Au air bridges. Figure 2 shows the cross-sectional view of the PIN MMIC technology.

Circuit Design

There are two fundamental switch configurations: series and shunt (figure 3). Many different combinations of these fundamental cells can be assembled. Our devices showed the best performance (i.e. on / off ratio) in the shunt configuration. Although additional cells (shunt or series) were found to increase isolation, they also increase insertion loss beyond acceptable levels. One drawback in using the shunt configuration is that tuning is required to reduce the loading effects of the off channels that have forward biased PINs shunting the lines. Using a 1/4-wave line between the feed-point and the shunt diodes is the most convenient solution; however, this restricts the bandwidth of the MMIC. The schematic diagram for the SP3T shunt switch is shown in figure 4. Blocking capacitors are required to isolate the bias of one PIN diode from the others.

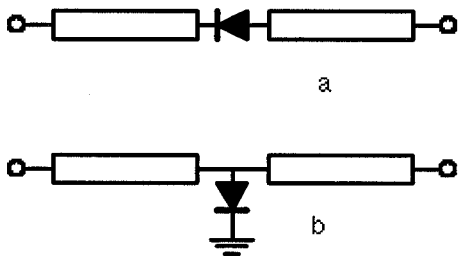

Figure 3. Fundamental PIN switch building blocks: series (a) and shunt (b). Series offers broader bandwidth but poorer isolation.

The design goals for the SP3T switch were < 2 dB insertion loss, > 20 dB isolation, > 15 dB return loss over the 70 to 80

GHz range. Since we use CPW for the circuit, a good model for the cross junction was needed. We used Sonnet software, a method-of-moments (MoM) electromagnetic (EM) simulator, to generate S-parameters for the 4-port cross junction. After estimating the required line lengths (total phase of 90° from cross junction to diode at 75 GHz, center of the band), an EM simulation of the entire switch was performed to verify that the estimated line lengths provide good return loss over the band of interest. A 2 pF MIM capacitor was formed in each of the 1/4-wave lines. Simulation results of the complete SP3T switch using the EM simulation of the CPW sections and the intrinsic device models are shown in figure 5.

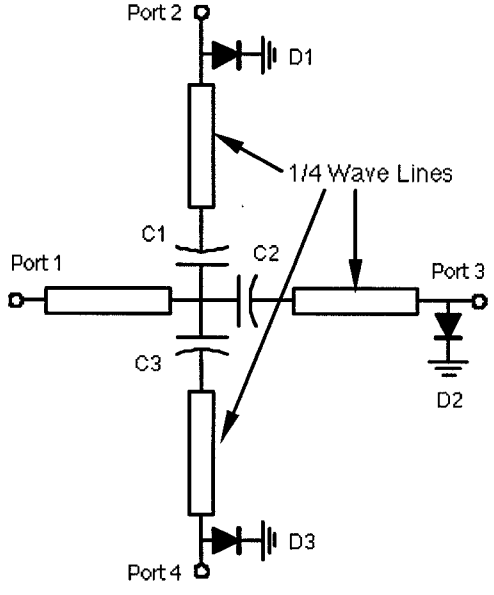

Figure 4. Schematic diagram of the SP3T GaAs PIN MMIC. Blocking capacitors are required to isolate bias.

Circuit Measurements

A photograph of the completed MMIC is shown in figure 6. On-wafer measurements were made using Picoprobe W-band wafer probes [3] that have integral bias-tees and a Wiltron 360 network analyzer (NWA) with W-band extenders [4]. The NWA only has two ports, so the other two ports were terminated with similar picoprobes having waveguide terminations. Our test setup was limited to the frequency range from 75 to 110 GHz. Referring to figure 4, the NWA is connected to ports 1 and 3. For the insertion-loss measurement, diodes D1 and D3 are forward biased at 15 mA, and diode D2 is reverse biased at 6 V. For isolation measurement, either diode D1 or D3 is reverse biased at 6 V, and the other diode and D2 are forward biased at 15 mA. The response of the MMIC is shown in figure 6. Measured insertion loss is < 1.5 dB, return loss is < 15 dB, and isolation is > 20 dB from 75 to 85 GHz.

Considering the center of the band is at 75 GHz, we expect the MMIC to have symmetrical performance in the 65 to 75 GHz range. Apart from the degradation in return loss away from the center frequency (due to 1/4-wave lines), the switch performs well across the entire W-band (we expect similar performance across V-band) with < 1.6 dB insertion loss and > 16 dB isolation. If one considers a return loss of 10 dB as the limiting case, the operating frequency range of the switch should be 50 to 100 GHz.

Conclusions

We have demonstrated a single-pole, triple-throw GaAs PIN diode CPW MMIC operating at W-band frequencies with < 1.5 dB insertion loss and > 20 dB isolation over the 75 to 85 GHz frequency range. To our knowledge, this is the first report of a W-band CPW SP3T switch with state-of-the-art performance. This technology is compatible with flip-chip mounting, and by implementing MMICs in the GaAs mate-

rial system without backside processing (CPW), low cost mm-wave functional blocks have been realized.

More isolation could have been achieved using an additional PIN diode in a series configuration to; but it would have increased insertion loss beyond acceptable levels for this application. Furthermore, coupling through the substrate may limit the maximum isolation obtainable in a CPW MMIC.

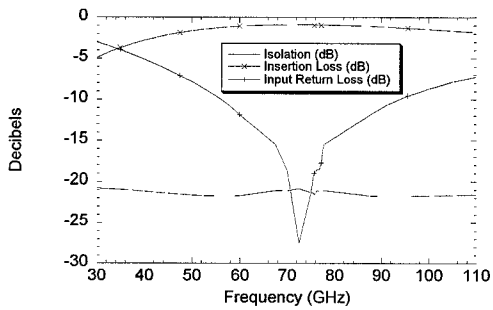

Figure 5. Simulated response of the SP3T PIN MMIC using EM simulated CPW structure and intrinsic device models. Simulated response indicates < 1 dB insertion loss, > 21 dB isolation over the 65 to 85 GHz range, and < 1.6 dB insertion loss and > 20 dB isolation from 50 to 100 GHz.

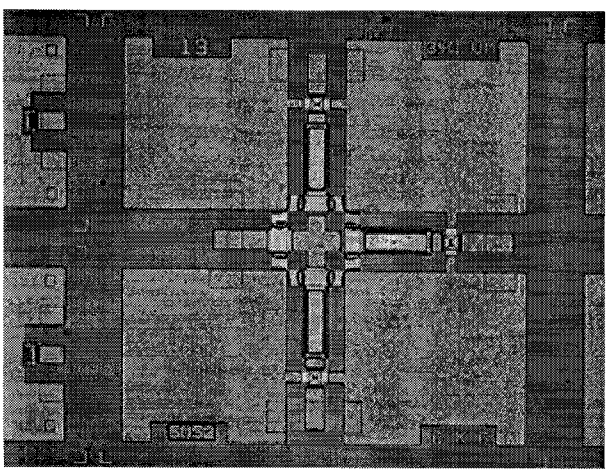

Figure 6. Photograph of the PIN MMIC. The input is fed at the left-hand port. Overall chip size is 1 X 1 mm^2. GaAs PIN devices and CPW transmission lines in combination with flip-chip mounting result in very low-cost MMICs.

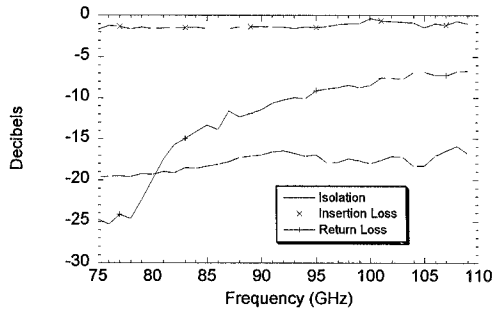

Figure 7. Measured response of the SP3T PIN MMIC. Available equipment limited measurements to 75 - 110 GHz range. Performance is expected to be symmetric about the center frequency (75 GHz). Measured insertion loss is < 1.5 dB, return loss is < 15 dB, and isolation is > 20 dB from 75 to 85 GHz, and insertion loss is < 1.6 dB and isolation is > 16 dB across the entire W-band (75 to 110 GHz).

References

[1] E. Alekseev, et al., "W-Band InGaAs/InP PIN Diode Monolithic Integrated Switches," 1996 IEEE GaAs IC Symposium, Orlando, FL, Nov. 1996.

[2] H. Takasu, et al., "W-Band Transistor Switches," Microwave and Guided Wave Letters, vol. 6, no. 9, Sept. 1996.

[3] Picoprobe by GGB Industries, Inc., P. O. Box 10958, Naples, FL 33941

[4] Anritsu Wiltron Company, 490 Jarvis Dr., Morgan Hill, CA 95037